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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/417,097	10/13/1999	MASAYUKI MASUYAMA	0819-298	6973

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MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/417,097	MASUYAMA, MASAYUKI	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *12-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/04/2005 has been entered.

Election/Restrictions

2. Applicant's election of Species I, corresponding to Figs. 3-10, read on claims 1-11, 22-25 in the reply filed on 6/17/04 is acknowledged.

3. Claims 12-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim.

The Applicant is reminded that upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Response to Arguments

4. Applicant's arguments with respect to claims 1-11 filed on 08/04/2005 have been considered but are moot in view of the new ground(s) of rejection.

In re page 11, Applicant argues that Wang discloses the row scanning shift register SR' only outputs the signals Q1 to Qm to the corresponding rows of R1-Rm of the array 19, and does not output any signal to the dummy pixel Rd.

In response, regarding claim 1, the Applicant amended claim with the limitation "the reset signal supplied from the reset signal supply means is output to pixels provided within an effective pixel area and dummy pixels that are provided in an area other than the effective pixel area." The Examiner considers that claim 1 as amended still does not distinguish from Kuroda in view of Wang et al.. Wang et al. discloses row injection means 33 as "reset signal supply means". Row injection means 33 outputs reset signals to the row or pixels R1 to Rm (effective pixel area) via reset switches RS1 to RSm, and reset signal to dummy row Rd via reset switch RSd, Figure 7, Column 12, Lines 42-53).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,512,543) in view of Wang et al. (US 4,862,276).

Regarding claim 1, Kuroda et al. discloses an amplifying solid-state imaging device comprising a plurality of pixels (pixels 32, figure 4, column 6, lines 11-25, column 4, lines 5-24) arranged in columns and rows, each said pixel including a signal storage section (photoelectric conversion/storage section 33, 6, lines 11-25, column 4, lines 5-24) for creating signal charge through photoelectric conversion and storing thereon signal information corresponding to the signal charge; reset signal supply means for generating a reset signal for an electronic shuttering operation and supplying the reset signal to the pixels belonging to one of the rows that has been selected to perform the electronic shuttering operation thereon, thereby resetting the signal storage sections included in the pixels on the selected row (reset transistors 80, figure 4, column 9, lines 15-65); row selecting means for sequentially selecting at least one row of pixels from the pixels to perform a signal readout operation thereon (shift register 36, selected-row-transistors 42, figure 4, column 9, lines 39-64); and a signal detector (driving transistors 35, load transistors 44, figure 4, column 9, lines 39-64) for reading out the signal information, which is stored in the signal storage sections included in the pixels on the row that has been selected by the row selecting means to perform the signal readout operation thereon, the signal detector including an amplifier (driving transistors 35, load transistors 44, figure 4, column 9, lines 39-64) that is connected in series between first and second power supplies (Vdd and Vss, figure 4), the signal detector sensing the signal information by making a current flow between the first and second power supplies, amplifying the signal information and then outputting the amplified signal information, wherein a period during which the reset signal supply means is supplying the reset signal to an arbitrary one of the pixel rows overlaps with a period during which the row selecting means is selecting another one of the pixel rows to perform the readout operation thereon (in

period 61, reset clock 81 to (n-1)th row overlaps with row selection 65 to nth row, during the period 61, when row (n-1)th is reset, row nth is selected to perform readout operation; and during the period 62, when row nth is reset, row (n+1)th is selected to perform readout operation; figure 5, column 9, lines 49-60, column 10, lines 16-32).

Kuroda fails to specifically disclose the reset signal supplied from the reset signal supply means is output to pixels provided within an effective pixel area and dummy pixels that are provided in an area other than the effective pixel area. However, Wang et al. teaches a push-pull readout array, which comprises an effective area (rows of pixels R1-Rm, figure 7) and dummy pixels (dummy pixels Rd, figure 7, column 12, lines 13-30), and row injection means 33 outputs reset signals to the row or pixels R1 to Rm (effective pixel area) via reset switches RS1 to RSm, and reset signal to dummy row Rd via reset switch RSd, Figure 7, Column 12, Lines 42-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Kuroda et al. by the teaching of Wang et al. in order to obtain an array in which the undesired pedestal in the array output waveform is eliminated (column 4, lines 53-55).

Regarding claims 2, 8, Kuroda et al. discloses the amplifier of the signal detector comprises drivers (driving transistors 35, figure 4) provided for the respective pixels; and load devices (load transistors 44, figure 4) provided for the respective pixel columns.

Regarding claims 3, 9, Kuroda et al. discloses each said driver (driving transistor 35, figure 4) is a transistor comprising a gate electrode (gate 34, figure 4) connected to associated

one of the signal storage sections (photoelectric conversion/storage section 33, figure 4); a drain connected to the first power supply (Vdd, figure 4); and a source connected to associated one of the load devices (load transistor 44).

Regarding claims 4, 10, Kuroda et al. discloses each said driver and associated one of the load devices together form a source follower circuit (column 6, lines 57-62).

Regarding claim 6, Kuroda et al. discloses wherein the number of the pixel rows is equal to an HD number, which is the number of horizontal sync signals included in one frame interval, disclosed as number n rows of imaging area 31 (number of pixel rows), and sequentially reading out nth row and (n+1)th row of imaging area 31 (the number of horizontal sync signals included in one frame interval, figure 4, column 9, lines 15-64, column 10, lines 15-32).

Regarding claim 7, Kuroda et al. fails to specifically discloses the pixels are classified into a group of imaging pixels that are provided within the effective pixel area and the dummy pixels, and wherein the number of pixel rows formed by the group of dummy pixels is obtained by subtracting the number of pixel rows formed by the group of imaging pixels from the number of the horizontal sync signals included in one frame interval. However, Wang et al. teaches a push-pull readout array, which comprises an effective area (rows of pixels R1-Rm, figure 7) and a group of dummy pixels (dummy pixels Rd, figure 7, column 12, lines 13-30), and number of pixel rows formed by the group of dummy pixels is obtained by subtracting the number of pixel rows formed by the group of imaging pixels from the number of the horizontal sync signals

included in one frame interval (figure 7). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Kuroda et al. by the teaching of Wang et al. in order to obtain an array in which the undesired pedestal in the array output waveform is eliminated (column 4, lines 53-55).

7. Claims 5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,512,543) in view of Wang et al. (US 4,862,276) further in view of Beiley et al. (US 6,522,357).

Regarding claims 5, 11, Kuroda et al. discloses each said signal storage section comprises a photodiode for performing photoelectric conversion (photoelectric conversion/storage section 33, 6, lines 11-25, column 4, lines 5-24).

Kuroda et al. and Wang et al. fail to specifically disclose a capacitor for storing thereon charge created by the photodiode; and a transistor for electrically connecting or disconnecting the photodiode to/from the capacitor. However, Beiley et al. teaches a CMOS image sensor, which comprises a plurality of pixels, each pixel comprises a capacitor 34 and a transistor (M2) 24, which connecting or disconnecting the photodiode 14 to/from the capacitor 34, figure 1, column 3, lines 19-35). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Kuroda et al. and Wang et al. by the teaching of Beiley et al. in order to store charge before read out. Doing so, the image quality of the readout image is increased.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T NGUYEN whose telephone number is (571) 272 - 7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WENDY GARBER can be reached on (571) 272 - 7308. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
08/15/05

LUONG T. NGUYEN
PATENT EXAMINER